An Advanced Single-chip Ka-band Transceiver

E. W. Lin, Y. Kok, G. S. Dow, H. Wang, T. T. Chung, S. Lau, D. Okamuro, B. R. Allen
TRW
Space and Electronics Group
Redondo Beach, CA

Abstract

This paper describes the development of an advanced single-chip Ka-band transceiver for military applications. The in-fixture measured performance of the transceiver chip will be presented. The transceiver chip monolithically integrates seven separate chips and one filter onto a single chip. In-fixture, the monolithic transceiver chip has demonstrated measured receiver noise figure of less than 6.5 dB across the RF band from 38.0 - 38.5 GHz at an IF of 2.45 GHz under -10 dBm LO drive. The transmitter output power was measured to be greater than 17.5 dBm across the 38.0 - 38.5 GHz band.

Introduction

In many military applications, it is essential to increase the reliablity of the electronic components. GaAs-based technology provides an opportunity to integrate many complex functions onto a single chip [1]. Such an implementation reduces human assembly errors by reducing the required number of chip-to-chip interconnections, and therefore increases system reliability. In addition, integration has great potential to reduce product cost. In this paper, we report on the development of a GaAs-based transceiver chip which monolithically integrates the front-end LNA, image-reject filter, mixer, IF amplifier, LO multiplier chain, and transmitter output driver amplifier.

Transceiver Chip Architecture

A block diagram of the transceiver chip, shown in Fig. 1, illustrates the degree of functional integration of the monolithic chip in a typical Ka-band digital transceiver sub-system. The receiving input begins with a two-stage, Ka-band balanced LNA which is followed by a single-stage single-ended buffer

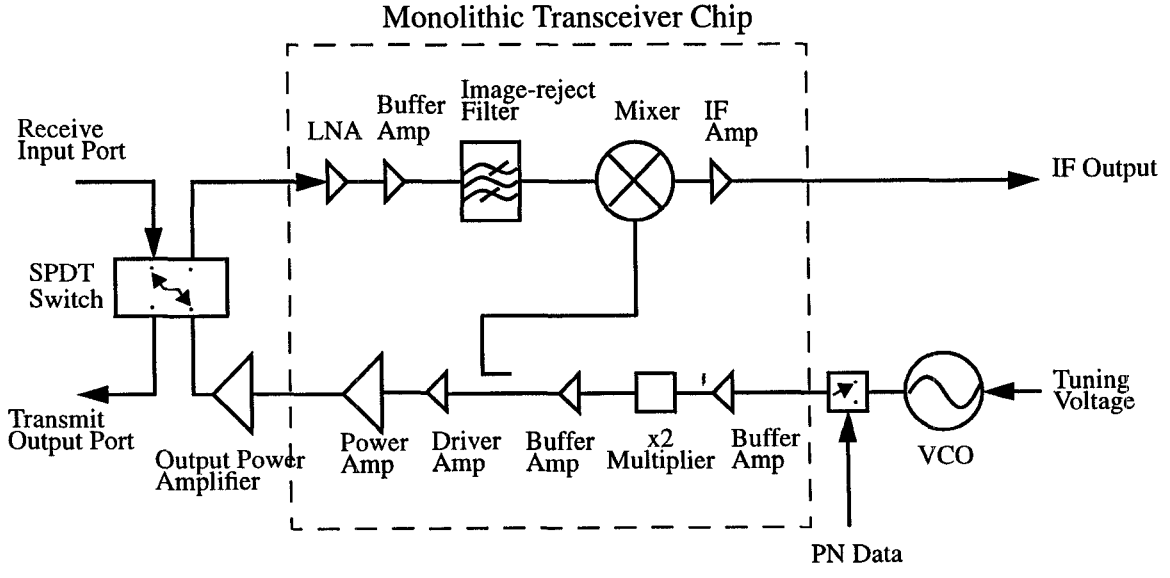

Fig. 1 Block diagram of a typical transceiver architecture illustrating integration of monolithic chip

This work was supported by the MIMIC Phase 2 Program (Contract No. DAAL01-91-C-0156).

0-7803-3246-6/96/$5.00 © IEEE

amplifier and an image-reject filter. The mixer utilizes a singly-balanced topology and uses dual HEMT gate-diodes as the mixing elements. The IF output of the mixer is extracted through a low-pass filter and is fed into a two-stage single-ended IF amplifier to output the S-band IF signal. At the LO input, two-stages of K-band amplification are followed by an active HEMT doubler which converts the K-band LO input to Ka-band. Next, four stages of single-ended amplification are used to increase the power level to allow the LO to be split to drive both the mixer and the output power amplifier chain. The output power amplifier chain consists of a single-ended pre-driver folowed by a balanced output driver amplifier. Separate bias inputs exist for the receiver side, LO transmitter chain, and output power amplifier. Fig. 2 shows a layout of the monolithic transceiver chip. The chip has dimensions of 4.5 x 5 mm^2 and has been fabricated using TRW's production GaAs pseudomorphic HEMT process [2].

Measured Performance

After on-wafer screening, the transceiver MMIC was been diced and mounted in a housing for fixture measurements. The conversion gain, noise figure, and output power results quoted below have all been corrected for fixture losses at the LO, RF, and IF ports. Fig. 3 plots the measured performance of the chip operated in its receiving mode and indicates that a noise figure less than 6.5 dB and conversion gain greater than 28 dB have been achieved across the RF band from 38.0 - 38.5 GHz under an LO drive of -10 dBm. The dc bias current consumed by the chip with +5 V applied to the receiver and transmitter bias

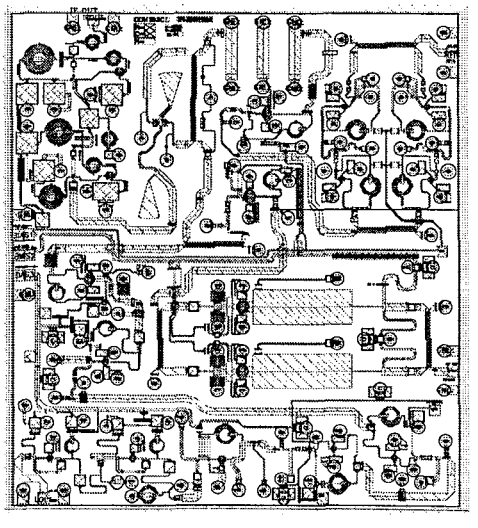

Fig. 2 Layout of the transceiver MMIC

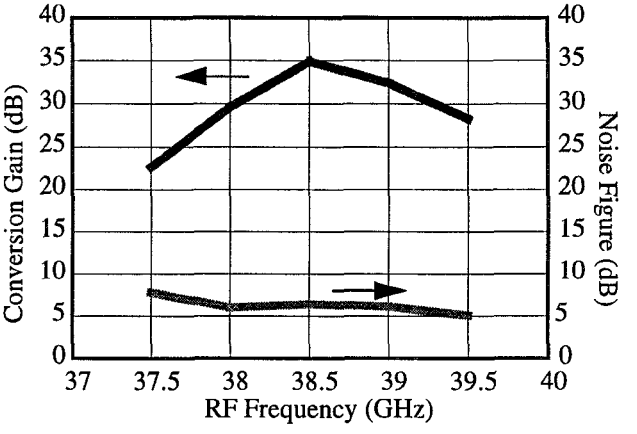

Fig. 3 In-fixture measured receiver conversion gain and noise figure of the monolithic transceiver chip with an LO input of -10 dBm

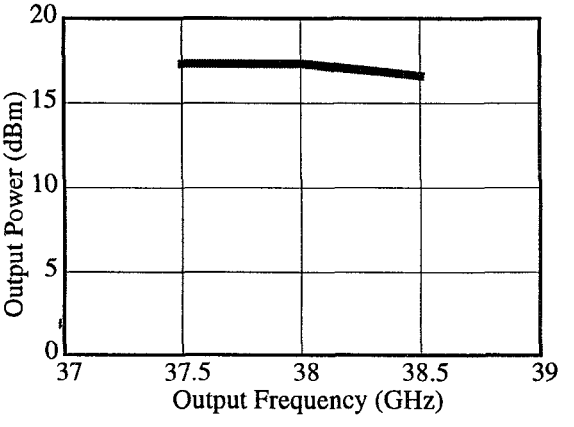

Fig. 4 In-fixture measured transmitter output power of the monolithic transceiver chip with an LO input of -10 dBm

inputs is nominally 320 mA.

Fig. 4 plots the output power from the transceiver transmit port over the frequency range 38.0 - 38.5 GHz. The maximum output power was measured to be greater than 17.5 dBm with an LO input of -10 dBm. The transmitter chain and output driver amplifier consumed 500 mA of current with +5 V at the bias inputs. In the IMA, the transmitter output of the transceiver chip will be used to drive a separate power amplifer chip.

Conclusion

The operation of a Ka-band monolithic transceiver chip has been successfully demonstrated. The chip has achieved conversion gain and noise figure of greater than 28 dB and less than 6.5 dB, respectively, across the receiving band of 38.0 - 38.5 GHz, and an output power of greater than 17.5 dBm across the transmitting band from 38.0 - 38.5 GHz. By combining several of the transceiver functions onto a single chip, we can easily insert the electronics into commercial or military systems, and the cost and manufacturing complexity of such systems have the potential to be dramatically reduced.

Acknowledgments

The authors would like to thank R. Kasody for his technical contributions and E. Barnachea for testing and the members of TRW's RF Products Center for their support.

References

[1] L. Tran, *et al.*, "Monolithic VCO and Mixer for Q-band Transceiver Using InP-based HBT Process," *IEEE 1995 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 101-104.

[2] R. Lai, *et al.*, "0.15 μm InGaAs/AlGaAs/GaAs HEMT Production Process for High Power and High Yield V-band Power MMICs," *1995 GaAs IC Symposium Digest*, p. 105.